in the data read step is set within the range where the drain-source current of the FET increases as the drain-source voltage of the FET increases. In other words, according to claims 1 and 2, since the voltage applied between the drain and the source is smaller than that applied to the gate of the FET, the drain-source current of the FET increases with the drain-source voltage. Accordingly, the lowering of the drain-source current with time can be suppressed, and the data retaining time or the retention characteristic can be improved.

The Examiner is respectfully directed to, e.g., page 13 lines 9-18 of the present specification wherein it can be understood that the magnitude of the data read voltage applied between the drain and source of the FET is in a non-saturated region.

Turning to the cited references, Taira teaches a MFS transistor and a MFMIS transistor, but completely fails to disclose the feature wherein the magnitude of the data read voltage applied between the drain and the source of the FET in the data read step is set within the range where the drain-source current of the FET increases as the drain-source voltage of the FET increases, as recited in claim 1. That is, Taira fails to disclose the magnitude of the data read voltage applied between the drain and source of the FET being in a non-saturated region.

Ishihara teaches a MFIS transistor. However, similarly to Taira, Ishihara completely fails to teach, disclose, or suggest the feature wherein the magnitude of the data read voltage applied between the drain and the source of the FET in the data read step is set within the range where the drain-source current of the FET increases as the drain-source voltage of the FET increases, as recited in claim 2.

In the Office Action, the Examiner asserts that, in the field of transistor design, it is considered inherent that within an operational bias range of a given FET, the current through the drain-source increase as the voltage applied across the drain-source increase. However, Applicants respectfully submit that this is a misunderstanding for the following reason:

Generally, since the FET is amplified by applying a voltage, which is higher than the gate voltage, between the drain and the source, even if the drain-source voltage increases, the drain-source current does not increase.
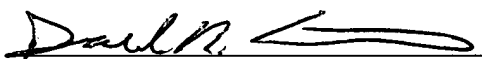
According to Fig. 5 and col. 6, lines 5-9 of Taira, since a same voltage (WL) is applied to the drain (42D) and the gate (43D), even if the drain-source voltage increases, the drain-source

NVA257780.2

current does not increase. Hence, Taira cannot have Applicants' claimed feature wherein the magnitude of the data read voltage applied between the drain and the source of the FET in the data read step is set within the range where the drain-source current of the FET increases as the drain-source voltage of the FET increases.

Again, as discussed above, both Taira and Ishihara fail to disclose or suggest that the magnitude of the voltage applied between the drain and the source is set within the range where the drain-source current increases as the drain-source voltage increases, and that the voltage applied between the drain and the source is smaller than that applied to the gate as recited in claims 1 and 2. Therefore, the pending §102(e) and the §103(a) rejections are improper. Accordingly, Applicants respectfully request reconsideration and withdrawal of the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,

Donald R. Studebaker
Registration No. 32,815

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, VA 22102
(703) 770-9300

NVA257780.2